Minimizing Electrostatic Charge Generation and ESD Event in TFT-LCD Production Equipment

Dong-Sun Kim (1&2)*, Chun-Bae Lim (1), Du-Seok Oh (1), Won-Joon Ho (1),
Ju-Young Jeong (1), Byeong-Hoo Park (1), Tae-Young Kim (2), Kwang S. Suh (2)

(1) Manufacturing Technology Center, LG Display, Paju-city, Gyeonggi-do, 413-811, Korea
tel.: 82-31-933-0120, fax: 82-31-933-0389, e-mail: kds815@lgdisplay.com

(2) Department of Materials Science and Engineering, Korea University, 5-1 Anan-dong, Seoul, 136-713, Korea

Abstract – This paper reports the results of investigations into electrostatic charging effects of a separation between glass and stage in TFT LCD manufacturing process. Generated electrostatic charge is closely related with vacuum pressure to hold the glass, holding times, separation cycles, and lift pin up height/speed. Therefore, effects on these factors are studied and a correlation between ESD damage and lift pin materials is analyzed. To avoid ESD damage and to minimize the charge generation during separation process, we suggest that the optimization of process condition and materials are required in addition to grounding and ionization.

I. Introduction

TFT-LCD displays are widely used in LCD TVs, notebook PCs, various flat monitors and portable electronic equipments such as mobile phones and tablet PCs. Since TFT-LCD device is composed of a number of layers and most of processes to integrate the layers involve movement, friction, and separation of glass substrate from various materials, the electrostatic charges are inevitably created during the manufacturing process [1]. The plate at LCD panel is a glass substrate with a transparent metal coating for the electrodes of the display. This insulating material can generate a high level of electrostatic charges and maintain the charges for quite a long time. The problem caused by static charge in LCD manufacturing faces with electrostatic discharge (ESD). Moreover, ESD problems become a critical issue as the thickness of glass substrate is in thinning trend.

During fabrication processes, the charge generation method and cause of static charge are various. Static charge is often generated by the friction from photoresist coatings applied to the glass surface and deionized water spray rinses used to clean the surface [2]. Both of these phenomena are well known as triboelectric charging including transferring processes by rollers or belts. Another method for charge generation is the pressure and separation of glass panels from vacuum chuck or stage. Generally, the number of contact and separation needed to more than 40 times to complete a panel. Whenever two surfaces in close contact are separated, one surface loses electrons and becomes positively charged, while the other surface gains electrons and becomes negatively charged. After separation, each surface retains its positive or negative charge, unless the surface is conductive and a path to ground is provided. This is the issue that grounding a glass substrate can not be a solution. Air ionization is recognized as the most effective means of neutralizing static charge on glass panel but is not enough to completely control the static charge [3]. The ESD event is related to static charge. So the best ESD protection solution is to minimize the charge generation during a variety contact and separation processes.

The purpose of this work is to study parameters of ESC in separation process from vacuum chuck with lift pin. Failure analysis of ESD damage is conducted to find out solution caused by contact materials involving separation. An influence of lift pin materials, which is closely related to ESD events, is analyzed. Also, we propose the effective way to minimize ESC generation during separation process in aspects of surface characteristics of stages and process conditions.

II. Problems and Failure Analysis

There happened severe yield loss caused by defects on the 8th generation glass. Figure 1 shows the failure defect location on a glass substrate. These defects are related with lift pin map.

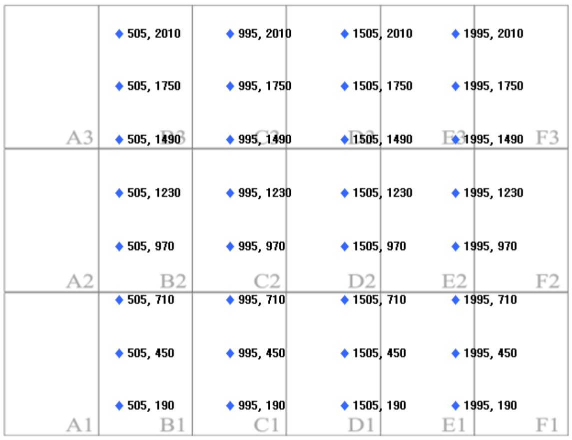


Figure 1: Failure defect information for analysis

In order to investigate the root cause of this failure, we analyzed the failure locations. The bottom metal is electrically and physically shorted as shown Figure 2(a) and (b). FIB cross-sectional view of the defect clearly shows the metal burnt and breakdown of insulating layer between the bottom metal and the upper metal as shown in Figure 2(c). The bottom metal is a gate line in transistors, so this burnt metal results in line defect, bright and dark spots failure. All the inspected failure samples have the same problems at same or very near around lift pins which directly contacted to glass.

Table 1: Lift pin resistance and ESD damage

Materials	Insulator (Silicon)	Dissipative (Vespel)
Surface Resistance (Ω)	1.0×10^{11}	$6.0 \times 10^{8} \sim 1.2 \times 10^{9}$
ESD Event	Not Seen	Often
Rockwell "E" Hardness (ASTM D-785)	20~30sh	12sh

Table 1 shows the electrical property of the lift pin. ESD damages on TFT glass occurred frequently in case of using dissipative lift pins but any damages were not observed when using insulative lift pins. The static dissipative materials are known for materials to prevent ESD damage and minimize charge generation, thus static dissipative lift pins had been adopted in electronic industry. However, using lift pins of dissipative materials is not proper solution for prevention of ESD event in separation process.

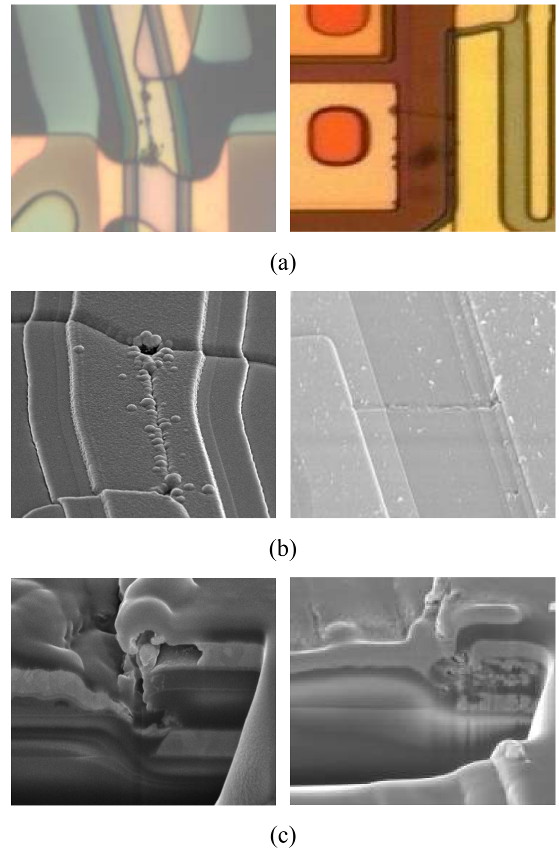


Figure 2: Physical failure analysis using (a) an optical microscope, (b) SEM and (c) FIB

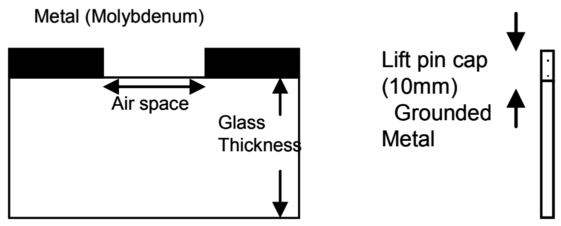
III. Experiments

A. Influence of lift pin materials

1. Experimental Procedures

To investigate a correlation between the ESD failure and resistance of lift pins, the canary pattern presented by Dupont Photomasks, which is vulnerable to ESD breakdown, was used as a sample [4]. Figure 3 shows the schematic of tested glass and lift pin. The Molybdenum canary patterns were fabricated on the 5th generation glass substrate. Air space gap was divided from 3㎛ to 10㎛ and glass thickness is 0.7㎜. For comparison of the frequency of ESD event, the split of pin resistance was arranged as shown in Table 2.

Figure 4 shows the ESD event test system. To reproduce a similar case with an actual process that charge generation mainly occurs at the backside of the glass, an upper glass was overlapped with the canary pattern glass so that induction voltage at canary pattern was applied symmetrically. High voltage power supply (205B, Bertan Inc.) was used for induction charging at metal layer of the canary pattern. Lift pin was approached to backside of the glass and then finally contacted. At each charging voltage from 1kV to 5kV with an incremental step of 0.5kV, 20 repetitive tests were conducted at each case. Finally, gap spacing of the canary pattern was observed using an optical microscope whether it was damaged or not.



(a) (b)

Figure 3: Schematic of test (a) glass and (b) lift pin

Table 2: Table 2. Resistance of lift pin cap

Resistance [Ω]	10^2	10^4	10^8	10^{10}	10^{11}
Material	SUS metal	PEEK Containing carbon	Vespel containing carbon	Vespel	PEEK

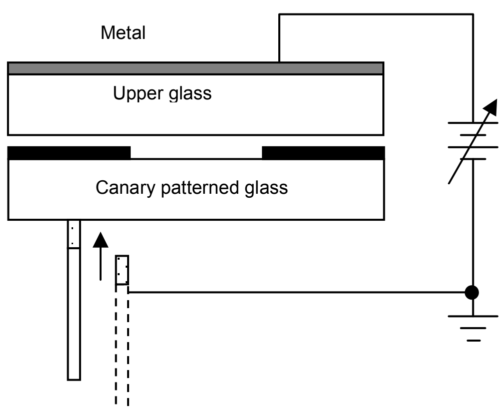
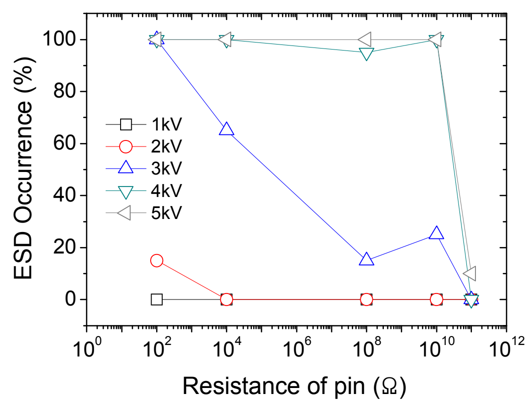


Figure 4: Test setup of ESD damage occurrence during lift pin contact

2. Results and Discussion

Figure 5 (a) shows the probability of ESD damage in samples with different resistances of lift pins. The probability of ESD occurrence was increased as increasing induction ESC on the sample. It is considered that the induction charge at metal layer becomes imbalanced by contacted lift pins on backside of glass. In other words, the pin contact induces additional generation of lateral electric field between an island and a guard ring of the canary pattern, resulting in a pattern breakdown. However, results show that the number of ESD occurrence is drastically reduced in case of using the 10^{11} **Ω**-contact pin. Therefore, using materials larger than 10^{11} **Ω** is desirable to prevent ESD events by lift pins. Figure 5 (b) shows minimal applied voltages to induce ESD damage samples with difference resistances of lift pins. As a similar vein, minimal applied voltage to induce ESD breakdown gets higher as using lift pins of the larger resistance. Also, the results show that minimal voltage to damage samples gets higher as pattern gap is wider. This result indicates that wider metal spacing needs larger differential voltage between two metals to damage patterns [5]. Therefore, designing wider metal spacing with consideration of overall layout is desirable to minimize ESD failures. Figure 5 (c) shows a breakdown image of the tested sample. Damaged layer at the gap spacing can be easily observed.



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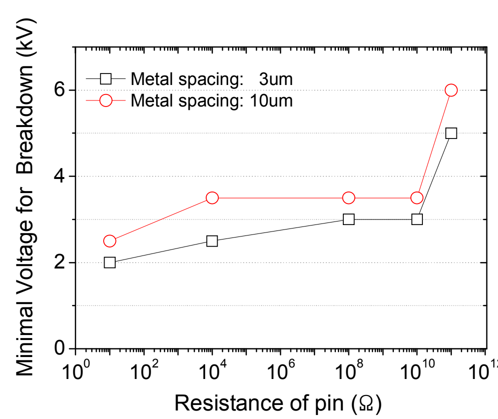

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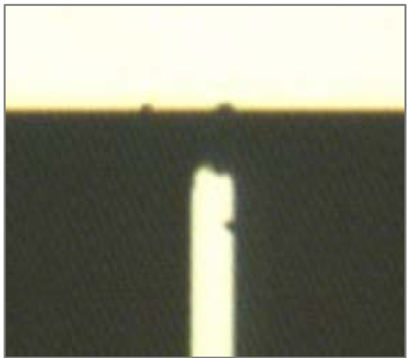


(c)

Figure 5: ESD damage occurrence with different (a) resistances of lift pins, (b) pattern gap, and (c) breakdown image at 3㎛ gap

B. Influence of stage materials and separation conditions

1. Experimental Procedures

To measure separation ESC values on glass from various stage materials, test equipment was used as described in Figure 6. Overall size of equipment was 5th generation (1100 X 1250 mm^2). An Ionizer was used to neutralize glass charges prior to tests.

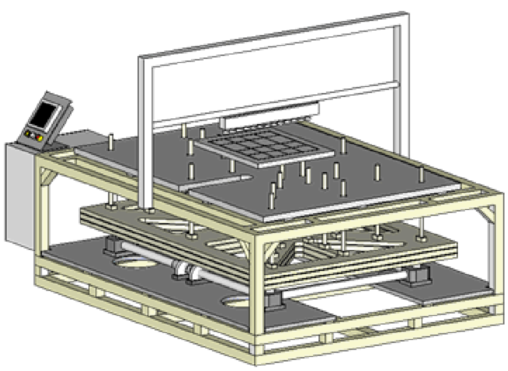


Figure 6: Stage equipment for glass separation test

Stage materials for tests were granite for mostly used on coater in photo lithography and Al_2O_3, SiC and quartz which is normally used for inspection tools. Teflon coated stage and CNT (Carbon Nano Tube) coated stage were also used. Surface resistance meter (PRS-801, Prostat Inc.) used to measure resistance of stages. Data recordable electrostatic voltmeter (542-2, Trek Inc.) was used to measure the charging voltages. Surface roughness tester (SJ-301, Mitutoyo Inc.) was also used. With these equipments, separation charging voltages were measured in accordance with variations of resistance, roughness and separation conditions of tested stages. All experiments was same conditions in controlled environment at temperature of 23±2˚C and relative humidity level of 50±5%.

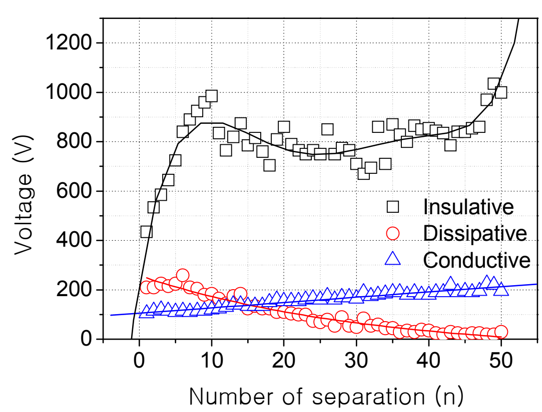
2. Results and Discussion

To investigate effects of stage materials, three stage materials with respective surface resistances were used. Used materials and each resistance are described in Table 3. Separation condition was identical for three stages. The conditions were pin up height of 150mm, lift pin-up speed of 300mm/sec, vacuum pressure of -0.8MPa and vacuum holding period of 30 seconds.

Firstly, separation ESC values in accordance with surface resistance were tested as shown in Figure 7 (a). In this test, bare glass substrates are used. Separation tests were conducted 50 repetitive times for all substrate and stages sets. The highest value was in case of using insulative stage materials and conductive surface resistance stage material was the lowest level at first hand. After 15 times of repetitive separation, the value of a dissipative stage material gets lower. These results agree well with basic electrostatic charge generations concepts. Figure 7 (b) shows the separation ESC values with different surface resistances using passivation layer deposited glass substrates. The results were different from prior tests. It was found that ESC values are some different from each film stack structure.

Table 3: Tested Stage Resistance Ranges

	Conductive	Dissipative	Insulative
Surface resistance (Ω)	10^4	10^6	10^{11}
Material	SiC	CNT Coating	Teflon Coating



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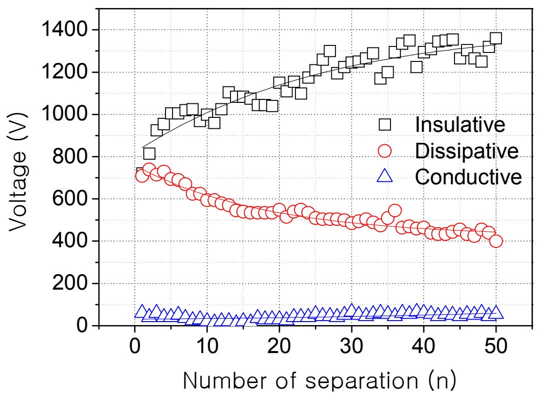


(b)

Figure 7: Charge generation results by stage material resistances in case of (a) bare glass, (b) passivation layer on glass

Figure 8 shows the ESC results as increasing the number of separation up to 150,000 times. A Teflon coated stage and metal patterned glass substrates were used in this experiment. ESC values are continuously increased even though ionization was conducted in every separation. This result is because of the residual static charges on high resistance stage. Therefore, both glass and stage surface must be neutralized by ionizers to prevent ESD damages and contaminations by electrostatic attraction.

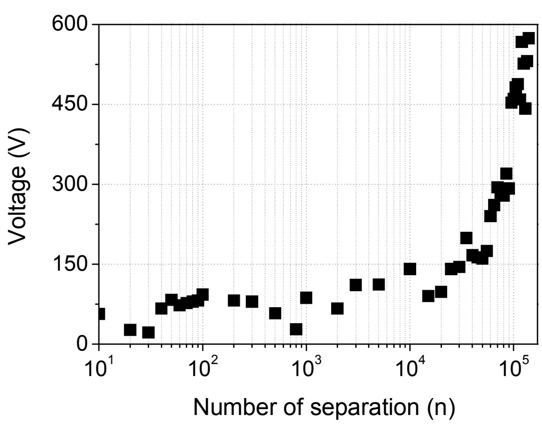


Figure 8: ESC values as increasing the number of separation up to 150,000 times

For the experiments on surface roughness of stages, granite stages with average roughness of 0.5, 1, 5 and 10 ㎛ were used, respectively. Separation conditions were same as prior tests. Figure 9 shows separation ESC values in accordance with surface roughness conditions. The charging voltages slowly get lower with increased surface average roughness of stages. This result indicates that increased roughness induce the reduced contact area between a glass and a stage. Accordingly, the amount of charge transfer was reduced.

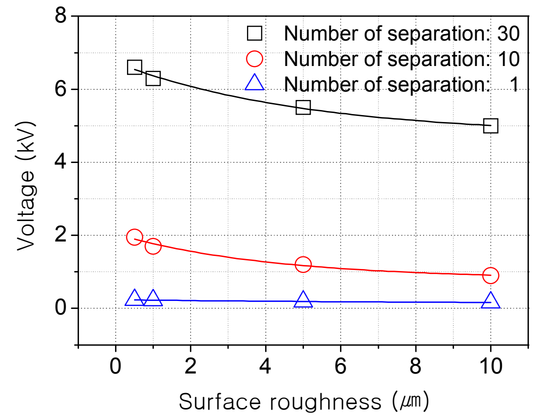


Figure 9: Separation ESC values on granite surface with different surface roughness

Table 4: Stage material properties

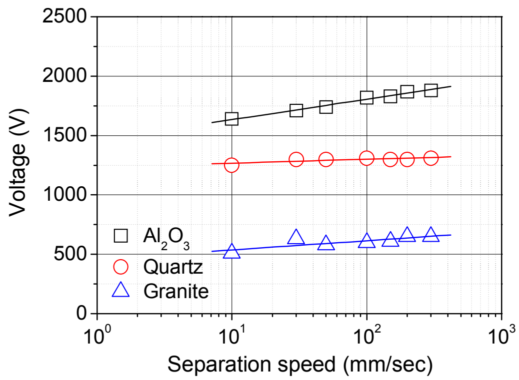
	Al_2O_3	Quartz	Granite
Surface resistance (Ω)	10^8~10^9	10^7~10^9	10^7~10^9
Volume resistance (Ω)	10^{14}	10^{11}~10^{13}	10^7
Surface roughness (㎛)	0.9~1.2	0.9~1.3	1.1~1.7

Major conditions on variation of separation charging are separation speed, vacuum pressure and vacuum time. To investigate effects of these separation conditions, test was conducted with Al_2O_3, quartz and granite stages. Table 4 shows properties of the test stages.

Figure 10 (a) shows the ESC values in accordance with the condition of separation speed. Increased ESC values were observed as increasing the conditions of separation speed but the variation of absolute numerical value was insignificant, especially at a quartz stage.

Figure 10 (b) and (c) shows the ESC values with different conditions of vacuum holding pressure and time, respectively. ESC values were increased as increasing vacuum holding pressure. This result can be inferred that increased vacuum pressure induces a larger contact area between a stage and a glass substrate, which is directly related to the amount of separation charge generation. Also, ESC values were increased as increasing vacuum holding time. This result is because of increased charge transfer time between a stage and a glass substrate. However, vacuum holding time can not be altered remarkably considering indeed process situations.

From these results, the variation vacuum pressure and surface roughness of stages are more effective. Therefore, minimizing vacuum pressure and increasing surface roughness with considering actual process conditions will be a proper solution.



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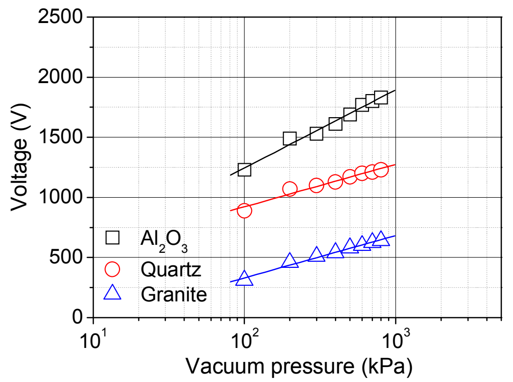

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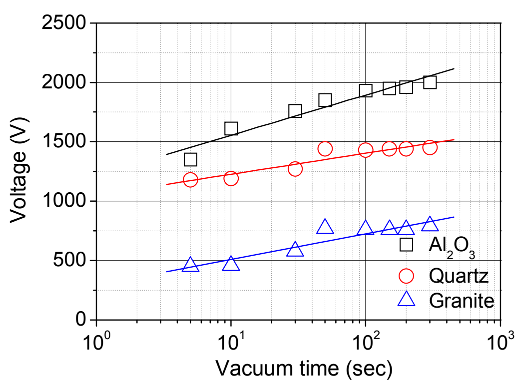

(c)

Figure 10: ESC values with different process conditions (a) separation speed, (b) vacuum holding pressures, and (c) vacuum time

IV. Conclusion

To minimize electrostatic charge and prevent ESD events on TFT LCD devices, static charge generation control is first effort by using ionizations to neutralize surface charges. From the results, both glass substrates and stages must be neutralized by ionizers to prevent ESD damages and contamination controls. Increasing surface roughness and minimizing separation speed and vacuum pressure is effective to control the charge generation of glass substrates. Using insulative materials instead of dissipative or conductive can prevent ESD events in case of glass contact parts. Furthermore, to prevent air discharge between glass and metal objects, proper distance or thickness of insulative materials is required in TFT LCD manufacturing processes.

References

[1] Tae Young Kim, Tae Hee Lee, Won Jung Kim, Jong Eun Kim, Kwang S. Suh, “Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer”, EOS/ESD Symposium 2008, pp. 191

[2] Toshio Murakami, Haruyuki Togari, Arnold Steinman M.S.E.E, “Electrostatic Problems in TFT-LCD Production and Solutions Using Ionization”, EOS/ESD Symposium 1996

[3] L. B. Levit, P. Gefter, “Ionization Applications and Pitfalls for Charge Neutralization in Substrate Handling”, EOS/ESD Symposium 2006-246, 4B.4-1

[4] Julian Montoya, Larry Levit, Andreas Englisch, “A Study of the Mechanisms for ESD Damages to Reticles”, Proceeding EOS/ESD Symposium, pp. 394-405, 2000.

[5] Steven H. Voldman, “ESD: Failure Mechanisms and Models”, John Wiley and Sons, Ltd, pp. 365-366, 2009